defines therewith at least one gap between said crystalline substrate and said at least one packaging layer, the crystalline substrate, microstructure and packaging layer forming a chip scale package,

the chip scale package having a multiplicity of electrical contacts plated along edge surfaces thereof.

39. A device according to claim 38 wherein at least one gap is located over said crystalline substrate and under said at least one packaging layer.

40. A device according to claim 38 wherein said packaging layer is sealed over said microstructure by means of an adhesive.--